The FE65-P2 Integrated Circuit

Version 1.1

Contents

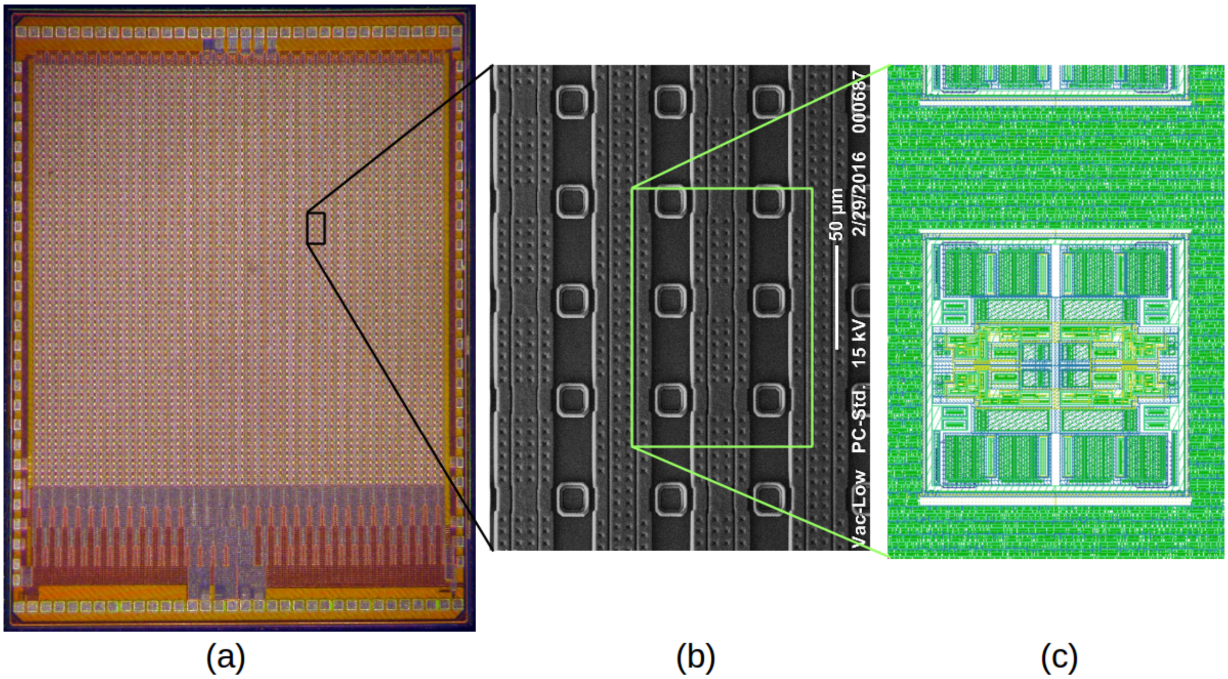

Figure 1: (a) Photograph of FE65-P2. References to bottom, top, left, and right throughout the text assume the orientation in this picture. (b) SEM micrograph showing detail with several bump pads on 50 μm pitch visible. The column power bus structure can also be seen. (c) layout detail showing an analog quad island surrounded by synthesized logic.

1 Introduction

This document is intended as both a user guide and a design reference to the FE65-P2 chip. The operation description is aimed at non-experts who will use the chip to carry out tests. Many details in this document will already be captured by existing test setup defaults. Descriptions of suitable test setups and software are not included here.

The FE65-P2 contains a matrix of 64 by 64 pixels on 50 μm by 50 μm pitch, designed to read out a bump bonded sensor. It is implemented in 65 nm bulk CMOS and was fabricated in a multi-project run delivered in December 2015. The goals of FE65-P2 are to demonstrate excellent analog performance, isolated from digital activity well enough to achieve 500 electron stable threshold, radiation hard to at least 500Mrad, and to prove the novel concept of isolated analog front ends embedded in a flat digital design, called analog islands in a digital sea. Each analog island is completely surrounded by digital circuitry, which was generated by automated place and route tools and will therefore be different around every island. A digital on top design flow was used, where each “quad column” of 4 by 64 pixels was synthesized as one unit. The chip outline is approximately 3.5 mm by 4.4 mm. Fig. 1 shows a chip photo, a layout view of an analog island, and an SEM image of the bump pad structure. The FE65-P2 design and test results are intended to inform the RD53A chip [1], which will be a large format prototype for the ATLAS and CMS Phase 2 pixel detectors.

Every FE65-P2 pixel has a dedicated analog front end, consisting of a charge integrator, followed by a single ended to differential second stage feeding a differential comparator. The front ends are laid out in compact groups of four or quads (also called analog islands) sharing power and bias distribution. Configuration bits for front end tuning and function selection are stored in the synthesized digital logic and supplied to each front end quad as static CMOS levels. Threshold discrimination is achieved by unbalancing the comparator differential inputs. Two global threshold DAC settings control this unbalancing. There are additionally 5 threshold trim bits in each pixel. The integrator has four gain choices selected by two global bits, and a current source feedback. There is a global adjustment for the feedback current, but no tuning bits on an individual pixel basis. The chip contains several variants for some of the front end details to be optimized, such as the values of the selectable feedback capacitors or presence of a pixel power down bit. Details about the analog front end and all variants are given in Sec. 2.

The FE65-P2 chip includes on-chip biasing circuitry, a simple serial programming interface and an output serial link allowing continuous triggering and data taking. The chip configuration has a hard-wired default value allowing standalone analog operation with minimal connections and no need for digital control, as summarized in Table 1. All control I/O not shown in Table 1 can be left unconnected as it contains internal pull-up/down resistors to set the default value. In particular, the 2-bit reset code is internally pulled to zero, which selects the default configuration.

For digital data acquisition operation the reset code must be externally controlled and a configuration loaded. It is not possible to use the default configuration of the pixel matrix while exercising the digital data acquisition. The basic digital operation requires just a few inputs and outputs as summarized in Table 2. The pixel matrix readout architecture is based on the FE-I4 region architecture [2] with some modifications, described in Sec. 3.

The FE65-P2 power and bias signal distribution have been optimized to minimize coupling and achieve low threshold. A column-based distribution is used for both, which necessarily crosses over "digital sea" in between analog quads. A metal layer is used as shield to prevent digital to analog coupling. All circuits, both analog and digital, are isolated from the substrate using well implant structures, while isolation of the I/O pads relies on a reverse-biased junction. This is why the substrate can be biased away from ground as indicated in Table 1 (this will be done only for special studies).

Symbol	Function	Min	Max	Comments
VDDD	Digital supply voltage	(VDDA-0.1) V $^{(*)}$	1.2 V	min. can be lower for testing
VDDA	Analog supply voltage	1.0 V	1.2 V	a single supply can be used
DAC_REF_VBN	Externally supplied master reference current (a.k.a Iref)	80 nA	120 nA	100 nA nominal. A resistor to VDDA can be used instead if performance is not critical
GNDD	Digital supply retrun	0 V	0 V	tie to common ground
GNDA	Analog supply retrun	0 V	0 V	tie to common ground
VSUB	substrate contacts	<-1 V	+0.2 V	nominally tie to ground
INJIN	Analog inject input	0 V	VDDA	falling edge injects
OUT_xx	Source follower pixel outputs	0 V	VDDA	must pull-up externally
IDDA	Analog current consumption	10 mA	18 mA	varies with Iref
IDDD	Digital current consumption	0	∼0 mA	
capA	Analog power decoupling	0.1 μF		
capD	Digital power decoupling	0.1 μF		
V_CTR_CF1/2	Feedback cap selection	0 V	VDDD	must be set- no internal pull-R

Table 1: Minimal requirements for basic analog operation. Power need only be supplied at one set of pads at the bottom of the chip, but multi-pin supply may improve performance. ($^{(*)}$ The analog quad configuration bits are supplied by the digital without level-shifting. Therefore too low a digital voltage relative to analog could lead to problems.

Symbol	In/Out	Function	Comments
Reset(0)	CMOS in	reset bit 0	set to 1 for full operation
Reset(1)	CMOS in	reset bit 1	set to 1 for full operation
SI_Config	CMOS in	shift register in	all configuration bits enter here
CLK_Config	CMOS in	shift register clock	advances the shift register
SO_Config	CMOS out	shift register out	
LD_Config	CMOS in	load global configuration	high loads SR contents, low latches
En_Pix_SR_Config	CMOS in	config. mode	set to load pixel column SR
TRIGGER	CMOS in	trigger gate input	gates CLK_BX to generate triggers
CLK_BX	CMOS in	bunch crossing clock	40 MHz nominal
CLK_DATA	CMOS in	data output clock	Must provide separately from CLK_BX. Up to 320 MHz
CLK_BX	CMOS in	bunch crossing clock	40 MHz nominal
OUT_DATA_P	CMOS output	8b/10b data	Yes, CMOS
OUT_DATA_N	CMOS output	inverted OUT_DATA_P	Not real differential

Table 2: Basic digital I/O connections needed for configuration and data acquisition

2 Analog front-end and variants

2.1 Front-end overview

The building blocks of the main array consist of so-called *quad-islands* of 2×2 pixels with custom analog pads isolated from the substrate hosting bias and power grids. No I/O, memory latches, flip-flops or counters are found in the analog portion of the pixel area; instead, static configuration values are provided by the digital core, which receives a comparator out signal from the analog part. This part is a small-area low-power front-end that has been designed for flexibility and testing. The ADC function is implemented using the time-over-threshold (ToT) principle, which is based on the fact that the comaparator pulse width is related to the amount of charge collected by the pre-amp. This enables evaluation of the charge collected by letting the counter in each pixel record the number of clocks for which the pulse remains above the discriminator threshold. The analog pixel just provides the discriminator pulse, while the counting is performed in the synthesized digital core.

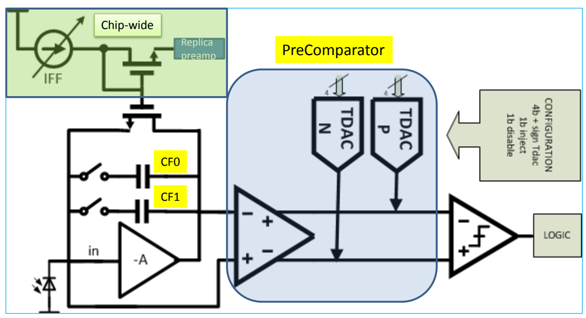

Figure 2: Block diagram of analog front-end.

When a particle passes through the sensor (diode symbol in the block diagram in Figure 2) it creates a certain amount of electron-hole pairs. These charge carriers will drift towards the charge-sensitive pre-amplifier and induce a signal at the input that it integrated by the amplifier. The pre-amplifier has a simple straight regulated cascode architecture (see Figure 3) in weak inversion and a first stage with continuous reset and adjustable gain through two selectable global bits. The pre-amp can operate at very low currents and has three bias lines. The pre-amp bias, voltage follower and feedback current settings are made through 8-bit global DACs. There is also a programmable injection capacitor (not shown in diagram) for analog calibration connected to the input of the pre-amp.

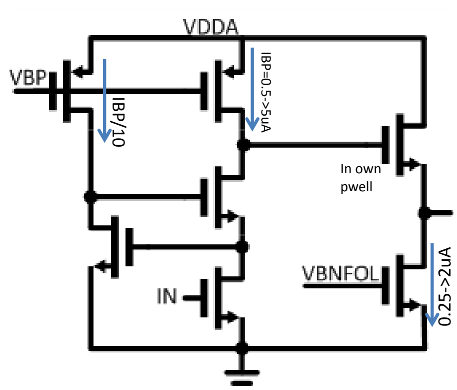

Figure 3: Pre-amplifier schematic.

The DC-coupled pre-comparator amplifier stage is also referred to as the differential threshold circuit. It implements threshold setting and tuning and provides additional gain. The global threshold is adjustable through two 8-bit DACs (vthin1 and vthin2) while the individual pixel thresholds can be adjusted by the pseudo-differential configuration of the two pre-comparator outputs that produces a differential signal at the input of the comparator by unbalancing signal levels. The added asymmetry feature of this unique design allows the pixel threshold to be fine-tuned by 4 + sign trim bits where the threshold (in e-) increases as the number represented by these 4 bits increases. The trim bits act on branch 1 or branch 2 of the differential threshold circuit for DTH1 and DTH2 respectively. This is done by threshold tuning DACs (TDACs) which provide a mechanism for making small relative threshold adjustments at the single channel level. The values of DTH1 and DTH2 are set by a single 5-bit pixel configuration register plus a global set bit value as detailed in Table 3. This design is optimized for low-threshold operation and allows the chip to be tested with both positive and negative charge carrier sensors as well as for the total area to be minimized. Other advantages include mismatch reduction and improved power supply rejection. The pre-comparator stage is followed by a classic CT comparator stage with output connected to the digital pixel region through logic gates.

Table 3: Truth table for the threshold tuning DACs. If the set bit value is 0 DTH1 will reflect the latch content and DTH2 takes the state of a global default line (0 or 15). If the set bit value is instead 1 DTH2 will reflect the latch content, while DTH1 takes on the default value.

5-bit DAC setting	Set bit value	DTH1	DTH2
0-15	0	0-15	0
16-31	0	0-15	15
0-15	1	0	0-15
16-31	1	15	0-15

Designed for 500e^- threshold operation, the analog pixel has a current consumption of 4 μA/pixel at 50 fF detector load and 10 nA leakage current, but is designed to operate up to 100fF load and 20 nA leakage, resulting in higher threshold and/or higher power. Assuming that power is anchored at 4 equidistant places, the maximum voltage drop provided by the power lines is ΔV$\sim$ 5 mV for a 336$\times$336 array at a current consumption of 5 μA per pixel. The target total analog current is below 5μA per pixel.

2.2 Analog variants

The FE65-P2 array is not completely uniform, but includes multiple circuit variants with varying properties in order to allow for testing and find optimal settings for the chip for different scenarios. At the core level the chip is partitioned into 16 quad columns (each quad column has 4 by 64 pixels), of which there are 8 variants (so there are 4 quad columns of each variety, see Figure 4). How this division has been implemented and specifications for each variant is described in Table 4a.

For CPLxx1 columns there is an additional feedback circuit such as the one displayed in the green box in the upper left corner of Figure 2, providing DC leakage current compensation through a low pass filter which increases the feedback gain (see Table 4a). The CPL011 variant is the only one with a power down setting, which is a new feature that has been added to allow powering down the analog activity.

There are no feedback current settings for individual pixels; instead, two globally switchable pre-amp feedback capacitances are used. Since this chip is a prototype, the value of these two capacitors can be varied in order to permit optimization for the final version of the chip. The values are set by the two control bits CF0 and CF1 and selected by jumpers on the test board to any combination of low/high referring to leaving the switches connected to the feedback capacitors open/closed respectively (see Table 4a for corresponding capacitor values). It is critical that these jumpers are always set to something (1 or 0), because there are not pullup or pulldown resistors on these pads and if left floating the feedback capacitance can vary randomly. The default baseline setting is to leave both switches open (i.e. CF0 and CF1 both set to low). In this case there will still be a non-zero feedback capacitance given entirely by parasitic capacitance, which is simulated to be ??? and which results in the highest gain.

Two of the column variants have an increased gate width of the amplifier PMOS load in order to improve the radiation hardness. These columns are marked ”RH” (see Table 4a).

In addition to the column variants, there are also 8 different top row test structures (see Table 4b and pin 90-101 in pinout table 7). These structures are used for injection of DC leakage current and to change the simulated detector capacitance externally with a varactor, which is a tuning diode used as a voltage-controlled capacitor ($\sim$ 70fF at 0V bias). This solution gives direct access to the buffered pre-amp output and the output between the first and second stage comparators. Each top row output goes to a source follower connected to an external pull-up resistor that can be used for probing the signal. Typical sample waveforms for a 500 mV peak-to-peak injection pulse are displayed in Figure **??**. (New waveforms to be added.)

Table 4: Variant partition.

Variant ID	CF0/CF1 [fF]	Power Dwn	Leakage Comp	W (amp2 load PMOS) [μm]	Column	Double column	Quad column
CPL000	3.36/4.99	no	no	0.2	0-7	0-3	0-1
CPL001	3.36/4.99	no	yes	0.2	8-15	4-7	2-3
CPL011	3.36/4.99	yes	yes	0.2	16-23	8-11	4-5
CPL001RH	3.36/4.99	no	yes	0.48	24-31	12-15	6-7
CPL100	5.15/7.76	no	no	0.2	32-39	16-19	8-9
CPL101	5.15/7.76	no	yes	0.2	40-47	20-23	10-11
CPL101RH	5.15/7.76	no	yes	0.48	48-55	24-27	12-13
CPL101	5.15/7.76	no	yes	0.2	56-63	28-31	14-15

(a) Column information. The binary naming scheme is such that the first digit (C) respresents the feedback capacitor values (low/high), the second digit (P) the power down feature (on/off) and the third digit (L) the leakage current compensation (on/off).

Column	Varactor	Leakage input
0-1	yes	yes
4-5	yes	yes
8-9	yes	yes
13-14	no	yes
14-15	no	yes
15-16	no	yes
16-17	yes	yes
20-21	yes	yes

(b) Top row information.

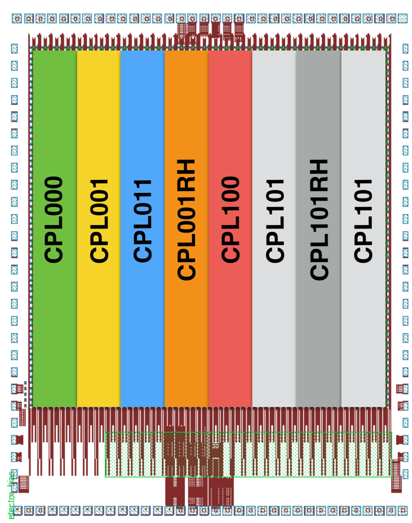

Figure 4: Illustration of analog FE column variants.

3 Region architecture

The discriminator output of each pixel is fed into a digital region where the firing time of each discriminator and the 4-bit ToT information is recorded from the counts of an externally supplied clock, with a nominal frequency of 40 MHz. Similar to the architecture of its predecessor FE-I4, the analog pixel matrix of FE65-P2 is divided into units of 2$\times$2 pixels and the digital readout with 25 ns time resolution is based on local hit storage in these quad regions. To deal with the high hit occupancies, each region has its own buffers and stores hit charge ($>$2GHz/s/cm^2) and timing locally for a programmable latency interval (up to 10μs) within which it can be retrieved by supplying an external trigger.

4 Configuration and control

The functionality of the chip is configurable through a serial peripheral interface (SPI) protocol slow control used to access the global and pixel registers (see Table 5 and Table 6 respectively). Threshold and bias values common to all pixels are set by DACs through the 145 bit global shift register. Additionally, each quad column has its own shift register that is 4x64 bits long. Configuration bits get serially clocked into the appropriate shift register and then transferred (loaded) in parallel to the actual configuration memories, which are separate from the shift registers (see Figure 5). There is a load signal (LD) to move bits from the global shift register to the global configuration memory, and 8 load signals to move bits from the pixel shift register to the pixel configuration memories (one load signal per bit). These pixel load signals are not separate inputs to the chip, but are controlled internally by bits in the global configuration. This is why there are two separate load signals for global configuration, so that the pixels can be configured without disturbing the global bias settings.

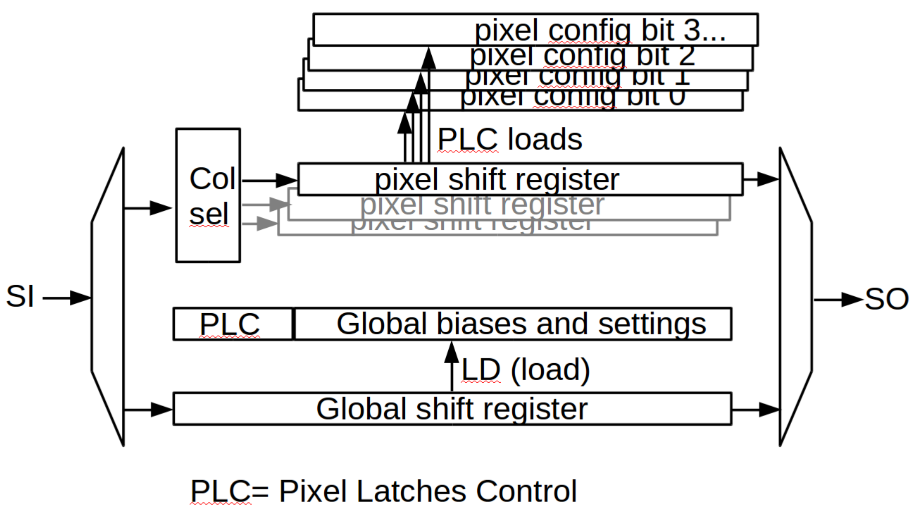

Figure 5: Configuration register data flow.

Table 5: Global registers

Start position (0 loads last)	Size (bits)	Name	Purpose	Default value
0	1	TestHit	Enable digital injection via LD_CNFG pin	Set bit
1	1	SignLD	Latch sign value into pixels	Set bit
2	1	InjEnLD	Latch inject enable into pixels	Set bit
3	4	TDACLD	Latch TDAC bits into pixels	4 × Set bit
7	2	PixLD	Latch 2 mode bits into pixels	4 × Set bit
9	1		Not used	
10	1	OneSR	Chain all shift registers into one	1
11	1		Not used	0
12	9	Latency	Trigger latency (in BX cycles)	400 (decimal)
21	16	ColEnable	Enable digital quad columns	0
37	16	ColSREnable	Enable quad column shift registers	FFFF (hex)
53	4	ColSROut	Select which pixel SR is sent to	15 (decimal)
57	8		Not used	0
65	8	PrmpVbp	Pre-amp bias	36 (decimal)
73	8	vthin1	Positive discriminator threshold	255 (decimal)
81	8	vthin2	Negative discriminator threhold	0
89	8	vff	Pre-amp feedback bias	42 (decimal)
97	8	VctrCF0	Not conncted	0
105	8	VctrCF1	Not connected	0
113	8	PrmpVbnFol	Pre-amp follower bias	51 (decimal)
121	8	vbnLcc	Leakage current compensation	1(decimal)
129	8	compVbn	Comparator bias	25 (decimal)
137	8	preCompVbn	Pre-comparator bias	50 (decimal)

Table 6: Pixel registers

Pixel	Bits	Default reset state	Comment
PixConf	[1:0]	b11	
InjCtrl	[0]	b1	
TDac	[3:0]	b1111	threshold tuning magnitude
Sign	[0]	b0	sign bit for the TDAC operation
SR (shif reg ff)	[0]	1(?)	used for digital inject mask (TestHitEn)

PixConf[1]	PixConf[0]	HitOrEn	HitEn	PowerOn
0	0	0	0	0
0	1	0	0	1
1	0	0	1	1
1	1	1	1	1

Figure 6: Nominal settings and specifications

Parameter	Description	Nominal	Comment
IBP	Preamp bias	2.0µA	Set by an 8b DAC. Can be overridden
IFF	Feedback bias	0.5µA	Set by an 8b DAC. Can be overridden
IBFOL	Follower bias	1.0µA	Set by an 8b DAC. Can be overridden
IPRECMP	Pre-comp bias	1.0µA	Set by an 8b DAC. Can be overridden
ICMP	Comparator bias	0.5µA	Set by an 8b DAC. Can be overridden
IBLCC	LCC amp bias	2nA	Set by an 8b DAC. Can be overridden
CFCTRL<1:0>	CF selection	00	OFF CHIP
vthn	Qth setting -	1.07V	Set by an 8b DAC. Can be overridden
vthp	Qth setting +	1.20V	Set by an 8b DAC. Can be overridden
InjectIn	Analog Injection	0.6V	OFF CHIP
CDET	Detector capacitance	0.1p	Maximum
ILEAK	Det. Leakage current	10nA	Maximum
HIT RATE	Hit rate	2GHz/cm2	Consensus?
In-time Qth	In time threshold	1000e-	100% efficiency?
Dble pulse res	Min. time between 2hits	500ns?	@10ke-? This determines the feedback setting.

Figure 7: Configuration settings

Name	Direction	Description
RESET[1:0]	input	Logic/Default GlobalConf/DefaultPixelConf
CLK_BX	input	BX clock (running continuously)
TRIGGER	input	trigger, synchronous to CLK_BX, active high
HIT_OR	output	hit or
CLK_CNFG	input	clock for configuration
EN_PIX_SR_CNFG	input	enable for configuring pixels (global<-> pixel SR)
LD_CNFG	input	load for configuration
SI_CNFG	input	data input for configuration
SO_CNFG	output	data output for configuration
PIX_D_CONF	input	selects default state of bits for D (in pixel)
CLK_DATA	input	clock for serial output data
OUT_DATA	output	output serial data

5 Readout

The digital logic is based on the preceding FE-I4 chip with additional memory to account for the increased hit rate and the digital core is built around the quad-regions, each with 7 memory buffers allowing storage of up to 7 hit arrival times for each region. Further, the digital part is divided into 64×4 super-regions, so-called *quad-columns* with 9-bit BCID memory (2×9-bit Gray counters) distributed for a more constant power consumption and reduced transients by eliminating local latency counters. These quad-columns are replicated 16 times in a step and repeat process to build the 64×64 pixel matrix (see Figure 8).

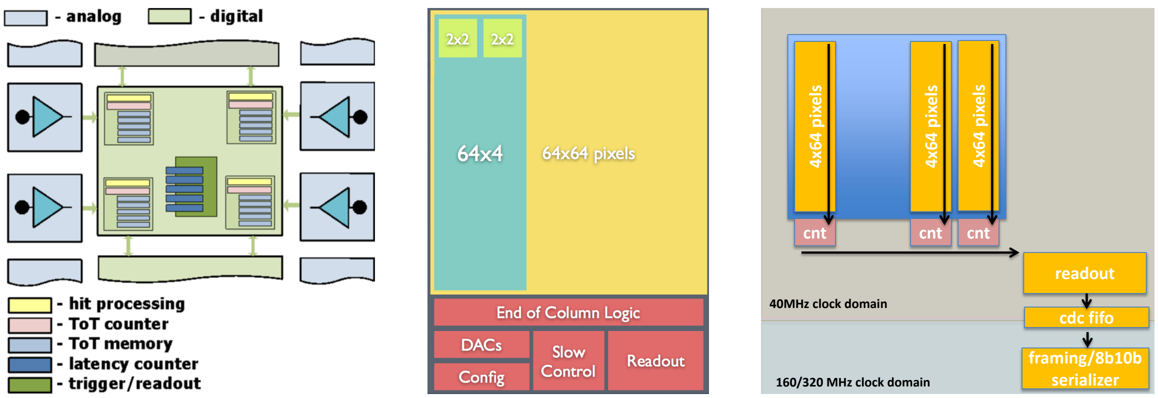

Figure 8: FE65-P2 digital layout and data flow.

The end-of-column logic hosts a token based trigger system and a 8b/10b high-speed formatter. The readout is based on a single token for the full chip and supports up to 16 consecutive triggers, with a default trigger rate of 1 MHz and a power consumption of 5.5μW/pixel. The pulse-height information is independently counted for each pixel by applying a digital threshold to the discriminator output prior to starting a dedicated 4-bit binary counter for ToT and using latches to store the distributed counter value. The information retrieved from individual pixels includes the address of the pixel, as well as the charge and timing information about the hit. The 24-bit word output data has the format: column, row, 2×ToT (see Figure 9).

Figure 9: Output data format

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
0	n/a	n/a	Column					Row					RowP	n/a	n/a	ToT0				ToT1			
1	BCID																						

The global signals are:

- bunch crossing clock
- 2×9 bit latency ID (distance of latency)
- 2×4 bit trigger ID/trigger request ID
- trigger

6 Pinout tables

The chip has several test pads along the periphery, which are yet to be routed for power, bias, and top row analog internal signals (see Figure 10). Information about the pinout and pads can be found in Table 7 and Table 8 respectively.

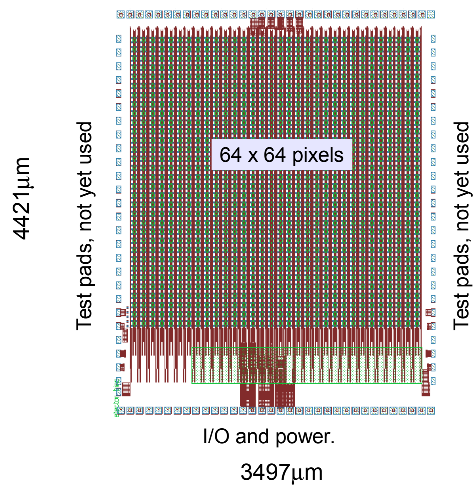

Figure 10: FE65-P2 pixel matrix structure.

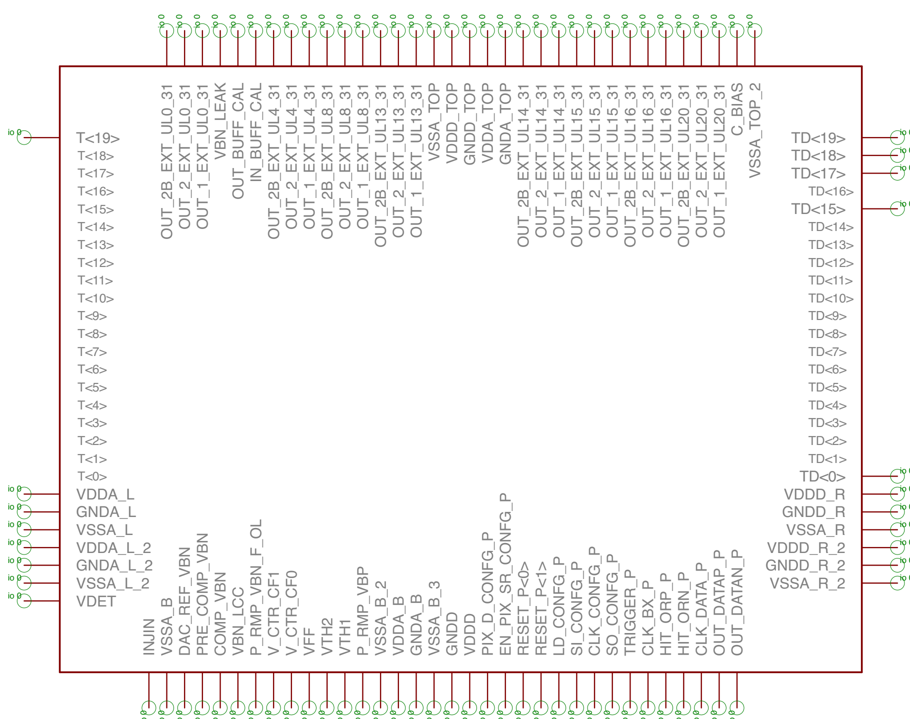

Figure 11: Pinout. References to the ”top”, ”bottom”, ”left” and ”right” are relative to this figure.

Table 7: Pinout information.

Pin#	Name	Description	Pin#	Name	Description
		Left (top→bottom)			Right (bottom→top)
1	T<19>	NC_ESD[a]	62	VSSA	substrate: 0V nominal [c]
2	T<18>	NC_ESD	63	GNDD	system ground: 0V (=GND)
3	T<17>	NC_ESD	64	VDDD	digital power: 1.2V[i]
4	T<16>	NC_ESD	65	VSSA	substrate: 0V nominal [c]
5	T<15>	NC_ESD	66	GNDD	system ground: 0V (=GND)
6	T<14>	NC_ESD	67	VDDD	digital power: 1.2V[i]
7	T<13>	NC_ESD	68	TD<0>	digital hit output; connect to std header pin. Disci out of pixel 63,7[b]
8	T<12>	NC_ESD	69	TD<1>	NC_ESD
9	T<11>	NC_ESD	70	TD<2>	NC_ESD
10	T<10>	NC_ESD	71	TD<3>	NC_ESD
11	T<9>	NC_ESD	72	TD<4>	NC_ESD
12	T<8>	NC_ESD	73	TD<5>	NC_ESD
13	T<7>	NC_ESD	74	TD<6>	NC_ESD
14	T<6>	NC_ESD	75	TD<7>	NC_ESD
15	T<5>	NC_ESD	76	TD<8>	NC_ESD
16	T<4>	NC_ESD	77	TD<9>	NC_ESD
17	T<3>	NC_ESD	78	TD<10>	NC_ESD
18	T<2>	NC_ESD	79	TD<11>	NC_ESD
19	T<1>	NC_ESD	80	TD<12>	NC_ESD
20	T<0>	NC_ESD	81	TD<13>	NC_ESD
21	VDDA	analog power: 1.2V	82	TD<14>	NC_ESD
22	GNDA	system ground: 0V (=GND)	83	TD<15>	NC_ESD[a]
23	VSSA	substrate: 0V nominal [c]	84	TD<16>	NC_ESD
24	VDDA	analog power: 1.2V	85	TD<17>	digital hit output; connect to std header. Disci out of pixel 63,58[b]
25	GNDA	system ground: 0V (=GND)	86	TD<18>	digital hit output; connect to std header. Disci out of pixel 63,61[b]
26	VSSA	substrate: 0V nominal [c]	87	TD<19>	digital hit output; connect to std header. Disci out of pixel 63,63[b]
27	VDET	DC LV detector bias			
		Bottom (left→right)			Top (right→left)
28	InjIn	analog injection pulse (50Ω to ground)	88	VSSA	substrate: 0V nom.[c] 100nF decoupling caps[i]
29	VSSA	substrate: 0V nominal [c]	89	Cbias	Varactor bias[d]
30	dacRefVbn	analog ref. current input (100nA nominal)	90	out1Ext_ul20_31	Analog out. Buffered preamp out1 of top row and DCOL 20 left pixel. [e]
31	preCompVbn	pre-comparator bias voltage[f]	91	out2Ext_ul20_31	Analog out. Buffered preamp out2 of top row and DCOL 20 left pixel. [e]
32	compVbn	comparator bias voltage[f]	92	out2bExt_ul20_31	Analog out. Buffered preamp out2b of top row and DCOL 20 left pixel. [e]
33	vbnLcc	leakage compensation amp bias voltage[f]	93	out1Ext_ul16_31	Analog out. Buffered preamp out1 of top row and DCOL 16 left pixel. [e]
34	PrmpVbnFol	pre-amp follower bias voltage[f]	94	out2Ext_ul16_31	Analog out. Buffered preamp out2 of top row and DCOL 16 left pixel. [e]
35	VctrCF1	logic level control feedback pre-amp cap[g]	95	out2bExt_ul16_31	Analog out. Buffered preamp out2b of top row and DCOL 16 left pixel. [e]
36	VctrCF0	logic level control feedback pre-amp cap[g]	96	out1Ext_ul15_31	Analog out. Buffered preamp out1 of top row and DCOL 15 left pixel. [e]
37	vff	pre-amp feedback bias voltage[f]	97	out2Ext_ul15_31	Analog out. Buffered preamp out2 of top row and DCOL 15 left pixel. [e]
38	vth2	global threhold control voltage V-[h]	98	out2bExt_ul15_31	Analog out. Buffered preamp out2b of top row and DCOL 15 left pixel. [e]
39	vth1	global threhold control voltage V+[h]	99	out1Ext_ul14_31	Analog out. Buffered preamp out1 of top row and DCOL 14 left pixel. [e]
40	PrmpVbp	pre-amp main bias voltag??	100	out2Ext_ul14_31	Analog out. Buffered preamp out2 of top row and DCOL 14 left pixel. [e]
41	VSSA	substrate: 0V nominal[c]	101	out2bExt_ul14_31	Analog out. Buffered preamp out2b of top row and DCOL 14 left pixel. [e]
42	VDDA	analog power: 1.2V[i]	102	GNDA	system ground: 0V (=GND)
43	GNDA	system ground: 0V (=GND)	103	VDDA	analog power: 1.2V[i]
44	VSSA	substrate: 0V nominal [c]	104	GNDD	system ground: 0V (=GND)
45	GNDD	system ground: 0V (=GND)	105	VDDD	digital power: 1.2V[i]
46	VDDD	digital power: 1.2V[i]	106	VSSA	substrate: 0V nominal[c]
47	PIX_D_CONF_p	default pixel config. setting. CMOS INPUT [j]	107	out1Ext_ul13_31	Analog out. Buffered preamp out1 of top row and DCOL 13 left pixel. [e]
48	EN_PIX_SR_CNFG_p	enable/disable pixel (array) config. shift register	108	out2Ext_ul13_31	Analog out. Buffered preamp out2 of top row and DCOL 13 left pixel. [e]
49	RESET_p<0>	RESET bit 0[k]	109	out2bExt_ul13_31	Analog out. Buffered preamp out2b of top row and DCOL 13 left pixel. [e]
50	RESET_p<1>	RESET bit 1[k]	110	out1Ext_ul8_31	Analog out. Buffered preamp out1 of top row and DCOL 8 left pixel. [e]
51	LD_CNFG_p	config. shift register LOAD command; Pulled down; CMOS INPUT	111	out2Ext_ul8_31	Analog out. Buffered preamp out2 of top row and DCOL 8 left pixel. [e]
52	SI_CNFG_p	config. shift register data input; Pulled down; CMOS INPUT	112	out2bExt_ul8_31	Analog out. Buffered preamp out2b of top row and DCOL 8 left pixel. [e]
53	CLK_CNFG_p	config. shift register clock; Pulled down; Pulled down; CMOS INPUT	113	out1Ext_ul4_31	Analog out. Buffered preamp out1 of top row and DCOL 4 left pixel. [e]
54	SO_CNFG_p	config. shift register output[l]	114	out2Ext_ul4_31	Analog out. Buffered preamp out2 of top row and DCOL 4 left pixel. [e]
55	TRIGGER_p	trigger pulse; Pulled down; CMOS INPUT	115	out2bExt_ul4_31	Analog out. Buffered preamp out2b of top row and DCOL 4 left pixel. [e]
56	CLK_BX_p	BCO clock; pulled down; CMOS INPUT. Main system freq. 40MHz nom.	116	inBuffCal	Analog input to the calibration buffer used for the out signals
57	HIT_ORP_p	The OR of all chip hits (positive)[m]	117	outBuffCal	Analog output of the calibration buffer. Must be pulled up to VDDA.
58	HIT_ORN_p	The OR of all chip hits (negative)[m]	118	vbnLeak	Analog DC current injection input[n]
59	CLK_DATA_p	DATA CLOCK; Pulled down; CMOS INPUT; 160MHz nom. (320MHz max.)	119	out1Ext_ul0_31	Analog out. Buffered preamp out1 of top row and DCOL 0 left pixel.[e]
60	OUT_DATAP_p	DATA OUTPUT (positive)[o]	120	out2Ext_ul0_31	Analog out. Buffered preamp out2 of top row and DCOL 0 left pixel.[e]
61	OUT_DATAN_p	DATA OUTPUT (negative)[o]	121	out2bExt_ul0_31	Analog out. Buffered preamp out2b of top row and DCOL 0 left pixel.[e]

[a]Connected to ESD diodes only, NOT connected at PCB level. Should be connected to standard header pin. Not functional signal.

[b](0,0) is the lower leftmost pixel and (63,63) is the upper rightmost pixel.

[c]Do not connect to ground.

[d]Varactor simulates input capacitance for few select pixel on top row. See suggested PCB schemtaics.

[e]Must be pulled up to VDDA. See suggested PCB schematics. DCOL=double column. Pull up resitor is 750Ω nominal for all out1Ext_ulxx_31 and 1.5 kΩ nominal for all out2xExt_ulxx_31.

[f]100nF to ground. Lemo connector (to force current only if necessary).

[g]VDDA-signal-GND 3 std header pins.

[h] 100nF to ground. Lemo connector (to force voltage only if necessary).

[i]Needs decouplig caps to gnd. 4.7μF//100nF as close to chip as possible, 10nF close to every VDDx pad recommended.

[j]See the configuation sheet and RESET_p$<$0$>$ and RESET_p$<$1$>$.

[k]Pulled down; Pulled down; CMOS INPUT. See pad information in Table 8.

[l]Resistor in series recommended to reduce noise.

[m]CMOS OUTPUT ("differential"). Resistor in series recommended to reduce noise (value emprical $\leq$ 100Ω, start with 0Ω). Trace and load of HIT_ORP_p and HIT_ORN_p must be matched.

[n]To simulate leakage current for few select pixels. 100nF to gnd.

[o] CMOS OUTPUT ("differential"). Resistor in series recommended to reduce noise (value emprical $\leq$ 100Ω, start with 0Ω). Trace and load of OUT_DATAP_p and OUT_DATAN_p must be matched.

Table 8: Pad information.

	Name	Direction	Quantity	Position (0=leftmost)	Description
Digital domain	RESET[1:0]	input	2	2, 3	
	CLK_BX	input	0	9	BX clock (running continously)
	TRIGGER	input	2	8	trigger, synchronous to CLK_BX, active high
	HIT_OR	output	2	10,11	hit or
	CLK_CNFG	input	1	6	clock for configuration
	EN_PIX_SR_CNFG	input	1	1	enable for configuring pixels
	LD_CNFG	input	1	4	load for configuration
	SI_CNFG	input	1	5	data input for configuration
	SO_CNFG	output	1	7	data output for configuration
	PIX_D_CNFG	input	1	0	selects default state of bits for D (in pixel)
	CLK_DATA	input	2	12	clock for serial output data
	OUT_DATA	output	2	13, 14	serial output data
Analog/mixed domain	InjIn	input	1		(dynamic)
	PrmpVbp	input/output	1		
	vth1	input/output	1		
	vth2	output/output	1		
	vff	input/output	1		
	VctrCF0	input	1		(digital/analog)
	VctrCF1	input	1		(digital/analog)
	PrmpVbnFol	input/output	1		
	vbnLcc	input/output	1		
	compVbn	input/output	1		
	preCompVbn	input/output	1		
	dacRefVbn	input	1		
Other	VDDA		2		analog positive supply
	GNDA		2		analog ground
	VSSA (1)		2		analog negative supply
	VDDD		2		digital supply
	GNDD		2		digital ground

References

[1] RD53A specs

[2] Fei4 architecture